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Capacitance variability of short range interconnects

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Abstract End of the roadmap integrated circuit interconnects suffer from capacitance variability due to line edge roughness (LER), significantly impacting overall circuit performance. We forecast the capacitance variability of short range interconnects with realistic line edge roughness at the upcoming 45, 32, and 22 nm technology nodes using a fast TCAD capacitance tool. Capacitance variability is layout sensitive and worsens with reduction in feature size, and together with the increasing device variability requires inclusion in statistical models of standard cells from the 45 nm node onwards. If LER does not improve then, for example, by the 22 nm node, short parallel lines on metal 1 are predicted to have 12% variability and, depending on layout, SRAM bit line capacitance 7% variability.

Keywords Interconnect · Variability · Standard cell · Capacitance · 6T SRAM

1 Introduction

It is now accepted that the performance of end of the roadmap integrated circuit (IC) transistors are strongly affected by intrinsic parameter fluctuations [1]. Interconnects are now a key factor determining overall IC performance [2] and are analogously affected, through line edge roughness (LER). The causes of LER are well understood, arising

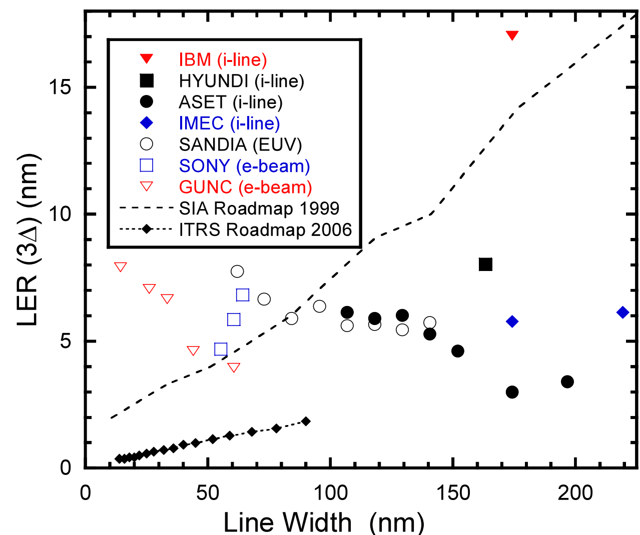

Fig. 1 Current and predicted line edge roughness (LER) [7]

primarily from polymer aggregation in the photoresist [3] leading to sidewall roughness that is faithfully transferred to the final structure upon etching [4]. There is a significant and worsening gap between the LER predicted by the International Technology Roadmap for Semiconductors (ITRS) and that currently realized by even the highest resolution electron-beam lithography tools, as shown in Fig. 1. Thus, LER-induced variability becomes increasingly important at upcoming technology nodes.

The influence of LER on the resistance of nanoscale lines has previously been studied [5], but the impact on the capacitance variability has not. Capacitance variability leads to variability in delay and power consumption. Due to the strong impact of interconnect on circuit performance, it is important to consider whether statistical models of standard

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cell behaviour should be extended to include not just transistor variability, but also the worsening problem of interconnect capacitance variability, and at what technology node.

This work aims to quantify the variability of the capacitance of short interconnects used within standard cells at the upcoming 45, 32 and 22 nm technology nodes.

2 Methodology

Two geometries are considered, as shown in Fig. 2, with parallel lines on M1 at minimum pitch of length up to 4 µm, as shown in Fig. 2a, and the bit lines in a standard 6T SRAM cell [6], as shown in Fig. 2b. Two ensembles of 800 structures were generated at each of the 45, 32 and 22 nm technology nodes, one with projected LER for that node (assuming improvement according to ITRS roadmap 2006) and one with current LER (assuming no improvement) as summarised in Table 1. In the case of the parallel metal lines in Fig. 2a line lengths of up to 4000 nm were considered, while the length of the SRAM lines in Fig. 2b was set by the scaled size of the SRAM cell (11.7λ).

The LER due to photolithographic and etch effects is modelled as a correlated line with a Gaussian power spectrum. The LER amplitude values for each technology node were taken from data in Fig. 1. The correlation length of the lines is chosen to be 20 nm [7]. Examples of the generated sidewall profiles are shown in Fig. 3 for the case of current and predicted LER.

In order to allow efficient exploration of a large parameter space, a well known empirical capacitance model for fast TCAD design synthesis of multilevel metal interconnects is employed [8]. This method outperforms competing empirical models [9], and is accurate to within 8% of measured data for complex three layer structures with crossovers. We expect improved absolute accuracy because we consider only a single layer structure and much higher relative accuracy because the empirical model and actual capacitance are both smoothly varying monotonic functions with less than 2% RMS fitting error. We have adapted the model to account for varying cross sectional dimensions due to LER in a manner analogous to that employed for the calculation of the capacitance of tapered interconnects [10]. Each track is discretised lengthwise into 1 nm sections. For each 1 nm section, the line-to-line and line-to-ground capacitances are calculated for an infinitely long ideal line having the same cross-section. A single ground plane (the substrate) is assumed, as shown in Fig. 4. The result is then scaled to 1 nm to give a per unit length capacitance, normalised to the unspecified effective dielectric constant ε_{ox} of the intervening material. In this way, the result remains applicable to interconnects with conformal dielectrics. The assumption of perfect conductivity in the metal lines does not affect the capacitance calculation.

The normalized line-to-ground capacitance for each discretised section of a single track is given by

$$\frac{C}{\varepsilon} = \frac{W}{H} + 3.28\left(\frac{T}{T+2H}\right)^{0.023} + \left(\frac{S}{S+2H}\right)^{1.16} \qquad (1)$$

where dimensions are width W, height H, distance above ground plane T, and separation to neighbouring tracks S [8]. The expression for the normalized line-to-line capacitance has a similar functional form but is omitted for the sake of brevity.

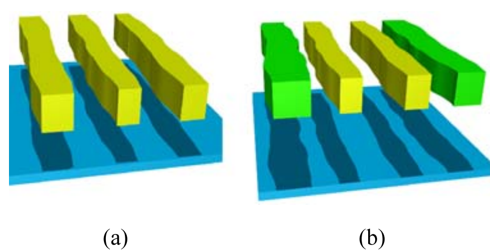

Fig. 2 Geometries studied in this work: **a** parallel traces on M1 at minimum pitch, **b** simplified 6T SRAM standard cell (bit and ground lines)

Table 1 LER (3Δ) (nm)

Technology	Improvement	No improvement
45 nm	1.4	3.0
32 nm	1.0	3.0
22 nm	0.7	3.0

3 Results

An example of the LER-induced variation of the normalised local capacitance components is shown in Fig. 5 for a 300 nm section of track (the illustration is for only two

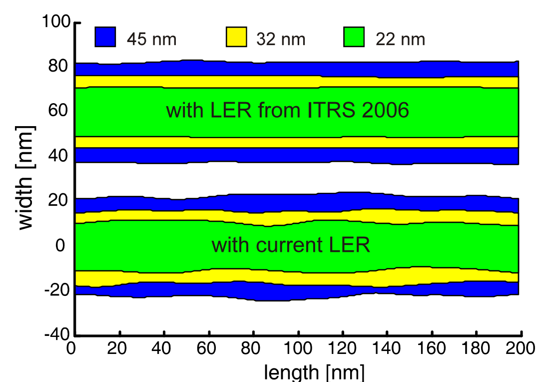

Fig. 3 Example sidewall profiles for current and predicted LER for 45, 32 and 22 nm technology nodes (to scale)

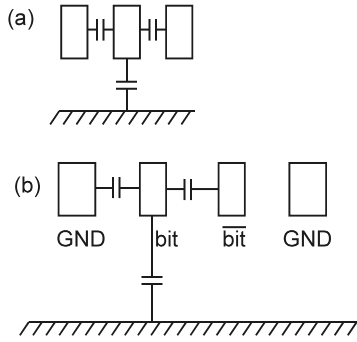

Fig. 4 Capacitances calculated for **a** parallel track on M1 at minimum pitch, **b** bitline in a simplified 6T SRAM cell

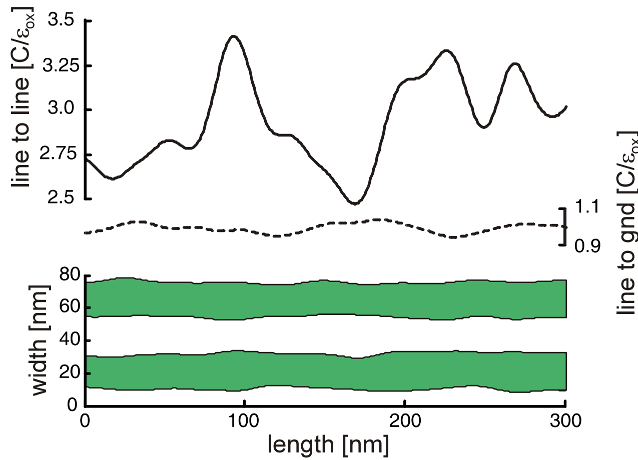

Fig. 5 Local variation in capacitance

tracks for the sake of clarity). The line-to-line capacitance contributes approximately 75% of the total capacitance and varies by 30% in the example shown in Fig. 5 because it is sensitive to the gap between the two tracks, increasing where the gap narrows and decreasing where it widens (e.g. at 90 and 170 nm along the length in Fig. 5 respectively). The line to ground capacitance is plotted for the lower of the two interconnect lines, and increases with increasing track width but is also influenced by the separation to the neighbouring track. The line to ground capacitance varies by less than 10% in the section shown.

The line length plays a significant role in determining the overall capacitance variability. For an ensemble of 800 parallel line structures (Fig. 2a), the $\pm 3\,\sigma$ capacitance variation is plotted in Fig. 6 as a percentage of the mean capacitance C_{mean} for a range of line lengths from 100 nm to 4000 nm (i.e. $6\sigma/C_{\text{mean}}$). While the longer lines exhibit small variability, significant variability of up to 12% can be expected at the shorter line lengths that are typically used within standard cells. The maximum variability is expected to drop below 2% if LER is improved to the ITRS requirement.

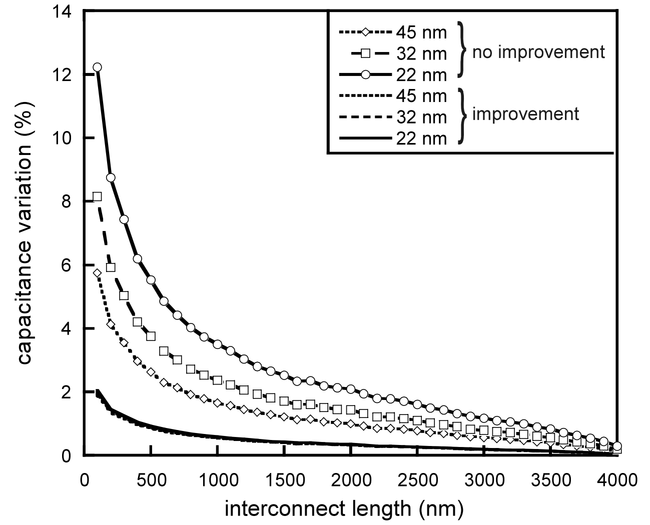

Fig. 6 Plot of capacitance variation as a function of interconnect length, for the 45, 32 and 22 nm technology nodes with and without improvement in LER

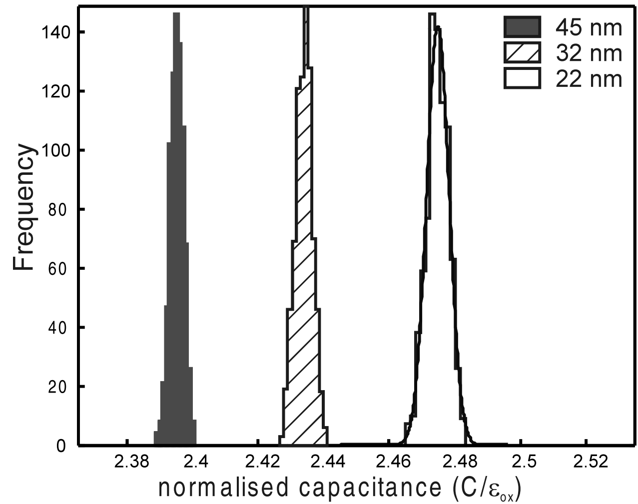

Fig. 7 Distribution of normalized bit line capacitance over ensembles of 800 6T SRAM structures for the 45, 32 and 22 nm generations respectively, assuming LER improves according to the roadmap

We further investigated the capacitance variation at short line lengths by studying interconnects within SRAM cells. For ensembles of 800 simplified SRAM structures, the distribution of the total normalised capacitance of the bit line is shown in Fig. 7 for the case where LER does improve according to the ITRS roadmap, and in Fig. 8 for the case where it remains at current levels. The $\pm 3\,\sigma$ variability for each of these ensembles is summarised in Table 2.

Variability is less than 1% if LER is improved, but ranges from over 1% at 45 nm to almost 5% at 22 nm if LER does not improve. Furthermore, the variability is sensitive to the cell layout. For example, halving the spacing between the bit lines to the minimum pitch increases the variability to just

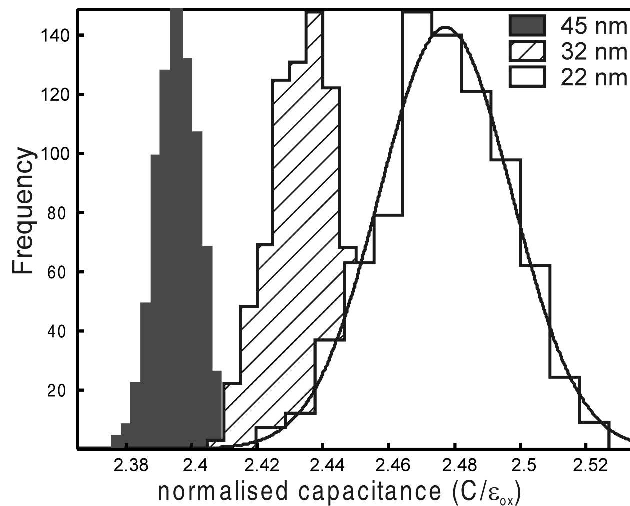

Fig. 8 Distribution of normalized bit line capacitance over ensembles of 800 6T SRAM structures for the 45, 32 and 22 nm generations respectively, assuming LER does not improve

Table 2 SRAM bitline capacitance variability

Technology	Predicted LER	Current LER
45 nm	0.53%	1.6%
32 nm	0.66%	2.7%
22 nm	0.82%	4.9%
22 nm*	1.2%	7.1%

* Reduced bit line spacing

over 7% at 22 nm. In all cases, the variability worsens as the critical dimensions shrink because the LER becomes larger relative to the nominal linewidth.

4 Conclusion

The capacitance variability due to line edge roughness was predicted for short range interconnects at the upcoming 45, 32 and 22 nm technology nodes using a fast TCAD tool. Ensembles of 800 structures were analysed, showing variability of up to 12% for short parallel lines on M1 at the 22 nm node, and just over 7% for SRAM bit lines depending on layout. Capacitance variability represents a significant, worsening problem if targets for LER cannot be met and additional sensitivity to layout parameters indicates the need for interconnect variability to be included in statistical models of standard cells from the 45 nm node onwards.

References

1. Samsudin, K., Cheng, B., Brown, A.R., Roy, S., Asenov, A.: Integrating intrinsic parameter fluctuation description into BSIMSOI to forecast sub-15nm UTB SOI based 6T SRAM operation. Solid State Electron. **50**, 86 (2006)
2. Meindl, J.D.: Interconnect opportunities for gigascale integration. IEEE Micro **23**(3), 28–35 (2003)
3. Yamaguchi, T., Namatsu, H., Nagase, M., Yamazaki, K., Kurihara, K.: Nanometer-scale linewidth fluctuations caused by polymer aggregates in resist films. Appl. Phys. Lett. **71**(16), 2388–2390 (1997)
4. Namatsu, H., Nagase, M., Yamaguchi, T., Yamazaki, K., Kurihara, K.: Influence of edge roughness in resist patterns on etched patterns. J. Vac. Sci. Technol. B **16**, 3315–3321 (1998)
5. Steinhögl, W., et al.: Microelectron. Eng. **76**, 126–130 (2004)
6. Weste, N.H.E., Harris, D.: CMOS VLSI Design, 3rd edn. Addison Wesley, Boston (2005)
7. Asenov, A., Kaya, S., Brown, A.R.: Intrinsic parameter fluctuations in decananometer MOSFETs introduced by gate line edge roughness. IEEE Tran. Electron. Dev. **50**(5), 1254–1260 (2003)
8. Chern, J.-H., Huang, J., Arledge, L., Li, P.-C., Yang, P.: Multilevel metal capacitance models for CAD design synthesis systems. IEEE Electron. Dev. Lett. **13**, 32 (1992)
9. Tosik, G., Lisik, Z., Langer, M., Wozny, J.: Simulation of parasitic interconnect capacitance for present and future ICs. Proc. Int. Conf. Comp. Sci. **3514**, 607–614 (2005)
10. Cumming, D.R.S.: Improved VLSI interconnect. Int. J. Electron. **86**(8), 957–965 (1999)