

Question/Answers	Panelist
<i>Is the variability only a glitch or a major treat to scaling and integration?</i>	
A major threat, degrading performance, power and yield.	T. Hiramoto
It's another factor to add to the long list of technical "challenges" that make designing an IC ever more difficult and expensive.	S. Furber
A major threat to COST EFFECTIVE scaling & integration	L. Benini
Major threat, can change the cost/benefit balance of scaling	G. Ianancone
No comment	B. Dierickx
Both spatial and temporal random variability are major threat to standard design	A. Mercha
Neither a glitch nor a major threat, just a problem like many other we have to deal with...	A. Cathignol
<i>Who has to sort out the variability problems technology or design?</i>	
Technology. There will be no substantial circuit solution for the random variations.	T. Hiramoto
Neither! Well, both, actually, but mainly it will be an EDA tools problem.	S. Furber
Looking forward: technology ↓ - design↑	L. Benini
The whole technology/design chain at the moment of choice of a CMOS technology à Coping with variability has a cost at the technology level and at the design level, but it is the total cost that counts.	G. Ianancone
Depends. The lowest level that can tackle it. If technology can do it, yes please, but...	B. Dierickx
What can not be tackled at technology level should be done by design..	A. Mercha
Key differentiator for fabless companies who can access the right technology and foundry data.	
Technologies has to reduce variability, Designers have to deal with it the best they can (variability resistant devices), both have to work together for an accurate variability description in the models	A. Cathignol
<i>What is the most promising variability resistant device architecture/solution?</i>	
Intrinsic channel SOI MOSFETs with thin BOX	T. Hiramoto
This isn't really my area, but 130nm transistors still work pretty well!	S. Furber
do not see any "golden egg"... but I am not a device design guy	L. Benini
FDSOI. (FinFET is too sensitive to LER).	G. Ianancone
Not existing yet. It likely will be a device structure that is reproducible at atomic level. Devices are identical large molecules. CNT is only a modest step in that direction. This will require to abandon the litho approach. Think of self-assembly, bio or non bio-inspired.	B. Dierickx
FinFET, UT FD devices, ..	A. Mercha
Undoped devices with a good electrostatic control have been shown to be excellent at the variability level (e.g. Finfet, GAA)	A. Cathignol
<i>What is the most promising variability resistant design solution?</i>	
Back-bias scheme	T. Hiramoto
For memories: redundancy and ECC. For general logic: redundancy, fault-tolerant design, asynchronous design and GALS, monitors and knobs, ...there is no 'silver bullet'	S. Furber
Design-time statistical analysis & optimization + post-silicon calibration (off-line & online)	L. Benini
For D2D variability, distributed process monitors and tuners	G. Ianancone
Largely mature: redundancy (of MEM) or design for matching Emerging: monitor/knob countermeasures, almost pure design / architecture solution Further away: Multi core systems having smart self re-scheduling and re-routing (GALS? Or not – e.g. fully A). This is almost a pure software & compiler based solution.	B. Dierickx
Correlation, Feed back control, Redundance	A. Mercha
I don't know... but I would say it much depends on the design we speak about; design is art and tailor made solutions are usually the best (at least for analog design)	A. Cathignol
<i>How the University based research can help with the variability problems.</i>	
Basic understandings of variability origins and Education	T. Hiramoto
By innovating 'outside the box'. By exploring novel devices, tools and architectures. By providing sound theories and models of variability. By helping train the next generation of engineers in these matters.	S. Furber
Teach statistical analysis & optimization techniques (math!) + Develop "design patterns" ... but industry has to share info (?)	L. Benini
As usual: Understanding and with new methodologies at the technology and design levels.	G. Ianancone
Excell where industry typically fails: Creative manpower (i.e. people have time to spend – does not	B. Dierickx

mean industry is not creative!) Out of the box thinking Set-up pre-competitive alliances Long term view, not hindered by next quarter numbers Explore novel device options (non SI, post Si). Check 10, keep 1, have 0.1 succeed... Explore novel SoC architecture options (...) Same for modeling, EDA...	
Training Masters & Phds in Statistical physics, Applied Statistics, Control theory, chaos, neural networks,...	A. Mercha
A good description of technological (physical) spread – Industry Physically based modeling - University	A. Cathignol